Abhishek Kumar Jain

Postdoctoral Research Staff Member, Center for Applied Scientific Computing
Lawrence Livermore National Laboratory (LLNL), USA

Livermore, CA, 94551
☎ *925.495.9525*
✉ *jain7@llnl.gov*
http://abhishekkumarjain.github.io/

Research Interests

- Architecture, compiler and runtime support for heterogeneous reconfigurable systems
- FPGA overlays for behavior-specialized acceleration of workloads on heterogeneous systems
- Throughput-oriented runtime programmable dataflow architectures
- Emulation of memory hierarchy and near-memory accelerators

Education

2012–2016 **Ph.D., Computer Engineering**, *Nanyang Technological University (NTU)*, Singapore.
Architecture Centric Coarse-Grained FPGA Overlays. Advisors: Douglas L. Maskell and Suhaib A. Fahmy
NTU Research Scholarship (2012–2016)
Courses: Advance Image Processing, Advance Computer Architecture, Real Time DSP Design, Advance Topic in Convex Optimization, Computer-Aided VLSI System Design, Principles of Embedded Systems

2008–2012 **B.Tech., Electronics & Communication Engineering (ECE)**, *Indian Institute of Information Technology (IIIT)*, Allahabad, India.
University Silver Medalist: 2^{nd} *Rank in the ECE Department (CGPA: 9.44/10)*
Dissertation work carried out at STMicroelectronics, India
Relevant Courses: Data and File Structures, Image Processing, Computer Architecture, Digital Signal Processing, Embedded Systems, Digital VLSI Design, Microprocessor Programming, Digital Electronics

Research and Work Experience

Mar 2017–present **Lawrence Livermore National Laboratory**, *Postdoctoral Research Staff Member*.
- Emulation of memory hierarchy and near-memory accelerators
- Leveraging Zynq Ultrascale+ device for developing LiME-ZU+ (advanced version of LiME)
- Evaluation of near-memory associative indexing using LiME-ZU+ (LLNL LDRD Project)
- Linux support for LiME-ZU+ to allow execution of multithreaded applications running on multi-cores
- Non-intrusive capture of application memory traces for Exascale Computing Project (ECP)
- Advisors: Dr. Maya Gokhale and Dr. Scott Lloyd

Fall 2016 **School of Computer Science & Engineering, NTU, Singapore**, *Postdoctoral Research Fellow*.
- **Software-Hardware Communication on Xilinx Zynq**: Developed AXI compatible Scratch-pad Memory Architecture around the FPGA overlay (including Linux Drivers) and integrated within Xilinx Zynq platform followed by performance characterization.
- **Just in time OpenCL compilation framework for FPGA overlays**: Developed mechanism for compiling OpenCL kernels at runtime for FPGA overlays on Xilinx Zynq.

2012–2016 **Hardware & Embedded Systems Lab, NTU, Singapore**, *Research Scholar*.
- **FPGA Overlay Architectures**: Research and development of FPGA overlays, an approach for mapping high level description of compute kernel onto FPGA hardware that reduces compile times and raises the level of programming abstraction. Designed and implemented a family of overlay architectures (spatially programmable and throughput oriented) that maximizes application throughput through the use of an array of DSP block based fully pipelined functional units and island-style routing network.
- **Tool-chain development for compiling C description onto Overlay architectures**: Software tool development, specifically for application mapping onto coarse-grained overlay architectures, including DFG extraction from high level description (C/OpenCL kernels), technology mapping, placement and routing of technology mapped netlists onto island-style architectures.
- **FPGA Virtualization Project**: Developed mechanisms for FPGA Virtualization specifically in programmable SoC device (Xilinx Zynq), where FPGA can be used as a shared resource among tasks running on a general purpose processor. Led a team of total 16 students (over the span of four years) working on the RTL implementation, FPGA prototyping and tool-chain development.
- Reviewer: FCCM(2014,2015), FPL 2013, FPT(2013,2014,2015), ASAP(2013,2015), DATE 2015

2013–2015 **School of Computer Science & Engineering, NTU, Singapore**, *Teaching Assistant*.
- CE2003: Digital Systems Design (2013, 2014, 2015)
- CE3001: Advanced Computer Architecture (2015)
- CE1005: Digital Logic (2015)

2013–2017 **School of Computer Science & Engineering, NTU, Singapore**, *MSc Dissertation Supervisor*.
- Sivasankaran Saranya (NTU MSc, 2013-14).
- Pranjul Singhai, Yue Shen, Manikandan Govindarajan, Syed Ali Asghar (NTU MSc, 2014-15).
- Prashant Ravi, Chetan Rathi, Uma Syam, Mu-Hua Hsieh (NTU MSc, 2015-16).
- Swarna Kamakshi, Abishek Sethupandi, Saurabh Adhikari, Deepshikha (NTU MSc, 2016-17).

Spring 2012 **STMicroelectronics, Greater Noida, India**, *Graduate Intern*.
- Project Title: Firmware library development for ARM Processor based STM32 Microcontroller.
- Developer for STM32 Microcontroller based Image Processing system (Optical Barcode Reader).
- Other projects included AES-CTR encryption, testing and validation of point of sale system.

Summer 2011 **University of Alberta, Edmonton, Canada**, *Summer Intern, MITACS Globalink Research Award*.
- Design and Simulation of MEMS based variable Capacitor using COMSOL simulation tool.
- Participated in Step workshops (Communication and Networking skills) organized by MITACS.

Skills

System Emulation	Modelling, simulation/emulation and evaluation of heterogeneous computing systems
Architecture	Comprehensive understanding of reconfigurable device architectures (Xilinx FPGAs and SoCs)
Design Tools	Experience with FPGA and SoC design tools (Xilinx ISE, XPS & SDK, Vivado, Vivado HLS
Programming	Fluent in C, C++/STL, SystemC, RTL Design and Verfication using Verilog HDL
Scripting	Proficient in Python and Shell scripting for Design Automation
Compiler	Familiar with OpenCL programming model, LLVM frontend (clang) and optimization passes

Research and Other Funding

Mar 2017-present **Co-I**, *Associative Indexing*.
PI: Maya Gokhale, LLNL, USA. Lab Directed Research and Development (LDRD) Project

Fall 2016 **Co-I**, *On-demand Hardware Acceleration of Cloud Services using FPGA Overlays*.
PI: Douglas L. Maskell, NTU Singapore. MOE Academic Research Fund (AcRF) Tier 1 Grant

2012-2016 **Research Scholar**, *NTU Research Scholarship*, $108,000.

Summer 2011 **Research Intern**, *MITACS Globalink Research Award*, $7,500.

Conference Talks

November 2017 **Supercomputing Conference (SC)**, *LiME: An Open Source Memory System Emulation Platform*, Workshop on Open Source Supercomputing (OpenSuCo), Denver, CO, USA.

November 2017 **Supercomputing Conference (SC)**, *The Role of FPGA Overlay Architectures in Exascale Computing*, Birds-of-a-Feather session on Reconfigurable Computing in Exascale, Denver, CO, USA.

May 2016 **Symposium on Field Programmable Custom Computing Machines (FCCM)**, *DeCO: A DSP Block Based FPGA Accelerator Overlay With Low Overhead Interconnect*, Washington DC, USA.

May 2015 **Symposium on Field Programmable Custom Computing Machines (FCCM)**, *Efficient Overlay Architecture Based on DSP Blocks*, Vancouver, Canada.

Invited Talks

May 2018 **Xilinx, Longmont, CO, USA**, *Architecture Centric Coarse-Grained FPGA Overlays* .

August 2016 **LLNL**, *Architecture Centric Coarse-Grained FPGA Overlays for High Performance Computing*.

May 2016 **Algo-Logic Systems, Santa Clara, CA, USA**, *Virtualizing FPGAs in Heterogeneous Computing Platforms using FPGA Overlays*.

May 2016 **Xilinx, San Jose, CA, USA**, *DeCO: A DSP Block Based FPGA Accelerator Overlay With Low Overhead Interconnect*.

Publications

Peer Reviewed Conference & Journal Papers

[1] Abhishek Kumar Jain, Scott Lloyd, and Maya Gokhale. Performance assessment of emerging memories through FPGA emulation. *IEEE Micro*, Under Review 2018.

[2] Abhishek Kumar Jain, Scott Lloyd, and Maya Gokhale. Microscope on memory: MPSoC-enabled computer memory system assessments. In *Proceedings of the IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)*, pages 173–180. Boulder, CO, USA, May 2018.

[3] Xiangwei Li, Abhishek Kumar Jain, Douglas L Maskell, and Suhaib A Fahmy. A time-multiplexed FPGA overlay with linear interconnect. In *Proceedings of the Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 1075–1080. Dresden, Germany, March 2018.

[4] Abhishek Kumar Jain, Xiangwei Li, Suhaib A Fahmy, and Douglas L Maskell. Adapting the DySER architecture with DSP blocks as an overlay for the Xilinx Zynq. *ACM SIGARCH Computer Architecture News (CAN)*, 43(4):28–33, September 2016.

[5] Abhishek Kumar Jain, Douglas L Maskell, and Suhaib A Fahmy. Are coarse-grained overlays ready for general purpose application acceleration on FPGAs? In *Proceedings of the IEEE International Conference on Pervasive Intelligence and Computing*, pages 586–593. Auckland, New Zealand, August 2016.

[6] Abhishek Kumar Jain, Xiangwei Li, Pranjul Singhai, Douglas L Maskell, and Suhaib A Fahmy. DeCO: a DSP block based FPGA accelerator overlay with low overhead interconnect. In *Proceedings of the IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)*, pages 1–8. Washington DC, USA, May 2016.

[7] Abhishek Kumar Jain, Douglas L Maskell, and Suhaib A Fahmy. Throughput oriented FPGA overlays using DSP blocks. In *Proceedings of the Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 1628–1633. Dresden, Germany, March 2016.

[8] Abhishek Kumar Jain, Suhaib A Fahmy, and Douglas L Maskell. Efficient overlay architecture based on DSP blocks. In *Proceedings of the IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)*, pages 25–28. Vancouver, Canada, May 2015.

[9] Abhishek Kumar Jain, Khoa Dang Pham, Jin Cui, Suhaib A Fahmy, and Douglas L Maskell. Virtualized execution and management of hardware tasks on a hybrid ARM-FPGA platform. *Journal of Signal Processing Systems (JSPS)*, 77(1-2):61–76, October 2014.

[10] Khoa Dang Pham, Abhishek Kumar Jain, Jin Cui, Suhaib A Fahmy, and Douglas L Maskell. Microkernel hypervisor for a hybrid ARM-FPGA platform. In *Proceedings of the IEEE International Conference on Application-Specific Systems, Architectures and Processors (ASAP)*, pages 219–226. Washington DC, USA, June 2013.

Workshop Papers

[11] Abhishek Kumar Jain, Scott Lloyd, and Maya Gokhale. LiME: an open source memory system emulation platform. In *Workshop on Open Source Supercomputing (OpenSuCo), at SC 2017*. Denver, CO, USA, November 2017.

[12] Abhishek Kumar Jain, Douglas L Maskell, and Suhaib A Fahmy. Resource-aware just-in-time OpenCL compiler for coarse-grained FPGA overlays. In *Proceedings of the Workshop on Overlay Architectures for FPGAs (OLAF), at FPGA 2017*. Monterey, CA, USA, February 2017.

[13] Abhishek Kumar Jain, Douglas L Maskell, and Suhaib A Fahmy. Coarse-grained FPGA overlays for on-demand acceleration of data center workloads. In *Second International Workshop on Heterogeneous High-performance Reconfigurable Computing (H^2RC'16), at SC 2016*. Salt Lake City, USA, November 2016.

[14] Xiangwei Li, Abhishek Jain, Douglas Maskell, and Suhaib A Fahmy. An area-efficient FPGA overlay using DSP block based time-multiplexed functional units. In *Proceedings of the Workshop on Overlay Architectures for FPGAs (OLAF), at FPGA 2017*. Monterey, CA, USA, February 2016.

Ph.D. Dissertation

[15] Abhishek Kumar Jain. *Architecture Centric Coarse-Grained FPGA Overlays*. PhD thesis, Nanyang Technological University, Singapore, August 2016.